

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Chee Hong Liao
Filed : Concurrently herewith
Title : Method of Processing Test Patterns for an Integrated Circuit

INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner for Patents,

Sir:

In accordance with 37 C.F.R. 1.98, copies of the following patents and/or publications are submitted herewith:

U.S. Patent No. 5,684,946 (Ellis et al.), dated November 4, 1997;

Zhao et al.: "Estimation of Switching Noise on Power Supply Lines in Deep Sub-Micron CMOS Circuits", IEEE, 13th International Conference on VLSI Design, January 2000, pp. 168-73;

Chakradhar: "Automatic Test Generation using Neural Networks", IEEE International Conference on Computer-Aided Design, November 7-10, 1988, pp. 416-19.

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications, patents and/or publications, it is because no existing translation is readily available to the applicant.

Respectfully submitted,

For Applicant

Date: July 18, 2003

Lerner and Greenberg, P.A.

Post Office Box 2480

Hollywood, FL 33022-2480

Tel: (954) 925-1100

Fax: (954) 925-1101

/bb

LAURENCE A. GREENBERG
REG. NO. 29,308

FORM PTO-1449 (SUBSTITUTE) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))				Attorney Docket No.: Applic. No. M&N-IT-465 Concurrently herewith Applicant _____ Chee Hong Liau Filing Date Group Art Unit July 18, 2003			
EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A	5,684,946	11/97	Ellis et al.			
	B						
	C						
	D						
	E						
	F						
	G						
	H						
	I						
FOREIGN PATENT DOCUMENT							
		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES NO
	J						
	K						
	L						
	M						
	N						
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)							
		Zhao et al.: "Estimation of Switching Noise on Power Supply Lines in Deep Sub-Micron CMOS Circuits", IEEE, 13 th International Conference on VLSI Design, January 2000, pp. 168-73.					
		Chakradhar: "Automatic Test Generation using Neural Networks", IEEE International Conference on Computer-Aided Design, November 7-10, 1988, pp. 416-19.					
EXAMINER				DATE CONSIDERED			
EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							